1. A method comprising:

initiating a direct memory access; and

successively transferring data from linked buffers in a first processor system to linked buffers in a second processor system.

2. The method of claim 1 wherein successively transferring data from linked buffers includes successively transferring data from buffers arranged in a linked list on a first processor system to buffers arranged in a linked list on a second processor system.

3. The method of claim 2 including providing descriptors that indicate the status of each of said buffers.

4. The method of claim 3 including providing flags that indicate whether a buffer is empty or full.

5. The method of claim 1 including transferring data between buffers in a cellular telephone.

6. The method of claim 5 including transferring data between a first processor system that includes a baseband processor and a second processor system that includes a multimedia processor.

7. The method of claim 1 including determining the status of a buffer to which data is to be transferred before transferring the data.

8. The method of claim 7 including determining if a buffer from which data is to be transferred is empty and if so, automatically filling the buffer with data.

9. The method of claim 8 including generating an interrupt when a buffer is empty and data is to be transferred from the buffer, intercepting the interrupt, and automatically filling the buffer.

10. The method of claim 9 including determining whether a buffer that is to receive data is full and if the buffer is full, automatically generating an interrupt, intercepting the interrupt, and automatically emptying the buffer.

11. An article comprising a medium storing instructions that enable a processor-based system to:

initiate a direct memory access; and

successively transfer data from linked buffers in a first processor system to linked buffers in a second processor system.

12. The article of claim 11 further storing instructions that enable the processor-based system to successively transfer data from linked buffers arranged in a linked list on a first processor system to buffers arranged in a linked list on a second processor system.

13. The article of claim 12 further storing instructions that enable the processor-based system to provide descriptors that indicate the status of each of said buffers.

14. The article of claim 13 further storing instructions that enable the processor-based system to provide flags that indicate whether a buffer is empty or full.

15. The article of claim 11 further storing instructions that enable the processor-based system to transfer data between buffers in a cellular telephone.

16. The article of claim 15 further storing instructions that enable the processor-based system to transfer data between a first processor system that includes a baseband processor and a second processor system that includes a multimedia processor.

17. The article of claim 11 further storing instructions that enable the processor-based system to determine the status of a buffer to which data is to be transferred before transferring the data.

18. The article of claim 17 further storing instructions that enable the processor-based system to determine if a buffer from which data is to be transferred is empty and if so, automatically fill the buffer with data.

19. The article of claim 18 further storing instructions that enable the processor-based system to generate an interrupt when a buffer is empty and data is to be transferred from the buffer, intercept the interrupt, and automatically fill the buffer.

20. The article of claim 19 further storing instructions that enable the processor-based system to determine whether a buffer that is to receive data is full and if the buffer is full, automatically generate an interrupt, intercept the interrupt, and automatically empty the buffer.

21. A system comprising:

a processor; and

a storage coupled to said processor storing instructions that enable the processor to:

initiate a direct memory access; and

successively transfer data from linked buffers in a first processor system to linked buffers in a second processor system.

22. The system of claim 21 wherein said storage stores instructions that enable the processor to successively transfer data from linked buffers arranged in a linked list on a first processor system to buffers arranged in a linked list on a second processor system.

23. The system of claim 22 wherein said storage stores instructions that enable the processor to provide descriptors that indicate the status of each of said buffers.

24. The system of claim 23 wherein said storage stores instructions that enable the processor to provide flags that indicate whether a buffer is empty or full.

25. The system of claim 21 wherein said system is a cellular telephone.

26. The system of claim 25 wherein said processor is a baseband processor, said system further including a multimedia processor.

27. The system of claim 21 wherein said storage stores instructions that enable the processor to determine the status of a buffer to which data is to be transferred before transferring the data.

28. The system of claim 27 wherein said storage stores instructions that enable the processor to determine if a buffer from which data is to be transferred is empty and if so, automatically fill the buffer with data.

29. The system of claim 28 wherein said storage stores instructions that enable the processor to generate an interrupt when a buffer is empty and data is to be transferred from the buffer, intercept the interrupt, and automatically fill the buffer.

30. The system of claim 29 wherein said storage stores instructions that enable the processor to determine whether a buffer that is to receive data is full and if the buffer is full, automatically generate an interrupt,

intercept the interrupt, and automatically empty the buffer.